IN THE CLAIMS

The current claims follow. For claims not marked as amended in this response, any difference in the claims below and the previous state of the claims is unintentional and in the nature of a typographical error.

1. (Currently Amended) A mixing circuit comprising:

one or more switching devices performing switching mixing of input signals with harmonic gating suppression of harmonic responses to the switching mixing, wherein at least one of the switching devices switches a first and a second differential transistor pair off for a period between each period during which one of the first and the second differential transistor pairs is switched on; and

a capacitive load coupled to the one or more switching devices and forming a low pass filter operating on an output of the one or more switching devices.

2. (Original) The mixing circuit according to claim 1, wherein the one or more switching devices comprise two differential transistor pairs controlled by local oscillator signals to perform the switching mixing and harmonic gating suppression.

3. (Currently Amended) The mixing circuit according to claim 2, wherein the local oscillator signals alternate switching a first differential transistor pair on for two periods in succession with switching a second differential transistor pair on for a single period~~, switching both~~

~~the first and second differential transistor pairs off for a period between each period during which one of the first and second differential transistors pairs is switched on~~.

4. (Original) The mixing circuit according to claim 1, wherein the capacitive load further comprises:

a network of switched load capacitors; and

an integration capacitor,

wherein the switched load capacitors integrate output current from the one or more switching devices for a period, sample an output voltage of the switched load capacitors following the period and transfer charge based on the sampled output voltage to the integration capacitor, and dump all accumulated charge.

5. (Original) The mixing circuit according to claim 4, wherein the network of switched load capacitors is controlled by signals having a clock frequency of two-thirds of a frequency of the output current and a duty cycle of one-third of a period of the output current.

6. (Original) The mixing circuit according to claim 1, further comprising:

switches demultiplexing a double sideband output signal from the one or more switching devices into a baseband output signal.

7. (Original) A receiver including the mixing circuit according to claim 1, the receiver further comprising:

a low noise amplifier coupling a received signal to the mixing circuit; and

at least one filter coupled to an output of the mixing circuit.

8. (Original) A communications system including the mixing circuit according to claim 1, the communications system further comprising:

a transmitter; and

a receiver including the mixing circuit and receiving a signal from the transmitter, wherein the mixing circuit operates on the signal received from the transmitter.

9. (Currently Amended) A method of operating a mixing circuit comprising:

employing one or more switching devices to perform switching mixing of input signals with harmonic gating suppression of harmonic responses to the switching mixing, wherein at least one of the switching devices switches a first and a second differential transistor pair off for a period between each period during which one of the first and the second differential transistor pairs is switched on; and

driving a capacitive load coupled to the one or more switching devices and forming a low pass filter operating on an output signal from the one or more switching devices with the output signal.

10. (Original) The method according to claim 9, wherein the one or more switching devices comprise two differential transistor pairs controlled by local oscillator signals to perform the switching mixing and harmonic gating suppression.

11. (Currently Amended) The method according to claim 10, wherein the local oscillator signals alternate switching a first differential transistor pair on for two periods in succession with switching a second differential transistor pair on for a single period~~, switching both the first and second differential transistor pairs off for a period between each period during which one of the first and second differential transistors pairs is switched on~~.

12. (Original) The method according to claim 9, wherein the capacitive load further comprises:

a network of switched load capacitors; and

an integration capacitor,

wherein the switched load capacitors integrate output current from the one or more switching devices for a period, sample an output voltage of the switched load capacitors following the period and transfer charge based on the sampled output voltage to the integration capacitor, and dump all accumulated charge.

13. (Original) The method according to claim 12, wherein the network of switched load capacitors is controlled by signals having a clock frequency of two-thirds of a frequency of the output current and a duty cycle of one-third of a period of the output current.

14. (Original) The method according to claim 9, further comprising:

demultiplexing a double sideband output signal from the one or more switching devices into a baseband output signal.

15. (Currently Amended) A phase alternating mixing circuit comprising:

an input stage receiving differential input signals;

a mixing stage receiving a differential input current representative of the input signals, the input stage comprising first and second differential transistor pairs switched under the control of first and second local oscillator signals, respectively, to perform switching mixing on the input current with harmonic gating suppression of harmonic responses to the switching mixing, wherein the first differential transistor pair is switched on for a first period, off for a second period, on for a third period, and off for a fourth period while the second differential transistor pair is switched off for the first, second and third periods and on for a portion of the fourth period equal to the first and third periods; and

a capacitive load coupled to the switching stage and forming a low pass filter operating on an output of the switching stage.

16. (Currently Amended) The phase alternating mixing circuit according to claim 15, wherein the first and second local oscillator signals producing a switching pattern in which

~~the first differential transistor pair is switched on for a first period, off for a second period, on for a third period, and off for a fourth period while the second differential transistor pair is switched off for the first, second and third periods and on for a portion of the fourth period equal to the first and third periods,~~

the fourth period includes~~ing~~ two periods equal to the second period during which both the first and second differential transistor pairs are switched off.

17. (Original) The phase alternating mixing circuit according to claim 16, wherein outputs of the first and second differential transistor pairs are cross-coupled, the first and second differential transistor pairs producing double sideband output signals.

18. (Original) The phase alternating mixing circuit according to claim 17, wherein the capacitive load further comprises:

first and second networks of switched load capacitors connected respectively to first and second outputs of the mixing stage, the first and second networks switched by signals having a clock frequency of two-thirds of a frequency of the double sideband output signals and a duty cycle of one-third of a period of the double sideband output signals; and

integration capacitors each connected to one of the first and second outputs of the mixing stage.

19. (Original) The phase alternating mixing circuit according to claim 18, further comprising:

switches demultiplexing the double sideband output signals from the one or more switching devices to produce a baseband output signal.

20. (Original) The phase alternating mixing circuit according to claim 19, wherein each network of switched load capacitors includes three capacitors.